

# Brad Meacham

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## Professional Objective

Seeking position as a Logic Verification Engineer using high level Verilog HDL, SystemVerilog, C/C++ based verification languages, and formal verification methodologies.

## Profile

ECAD engineer with over 20 years EDA experience using the Verilog language at gate, RTL, and behavioral level as well as the Verilog PLI and VPI extensions and logic design verification with the Verilog HDL and C/C++ based co-simulation.

## Professional Skills

**EDA Tools:** Verilog-XL, NC-Verilog, QuestaSim, Verilog PLI/VPI, SystemVerilog, Cadence TestBuilder, SystemC/SCV, Cadence Verification Cockpit, Cadence Incisive Simulation and Verification

**Software Languages, Programming Environments, Operating Systems:** C, C++, C Shell, Bourne Shell, Perl, Tcl, GCC, G++, Make, RCS, CVS, SunOS, Solaris, HP-UX, Linux, MacOS X, Windows 98/NT/2000/XP

## Professional Experience

### Simtek Corporation — Colorado Springs, Colorado — 2006 to 2008

#### Senior Staff Engineer in the Digital Design Group

- Primary responsibility included development of chip level self checking digital verification solutions for Simtek's 4-Mbit nvSRAM designs. Included development of reusable Verilog HDL simulation libraries.
- Provided general Verilog design and simulation support as needed for RTL designs.
- Designed and implemented design management and simulation methodologies using Make and scripts.

### Cadence Design Systems — Colorado Springs, Colorado — 2001 to 2003

#### Technical Education Specialist in the Educational Services Group

- Primary responsibility included development and delivery of customer training materials for Verification Cockpit, Incisive Verification, and TestBuilder. This included tools for Transaction Based Verification, Assertion Based Verification, Functional Coverage, Code Coverage, Transaction Analysis, and C/C++ co-simulation.
- Also responsible for delivery of both basic and advanced Verilog customer training courses.

### LSI Logic Corporation — Colorado Springs, Colorado — 2000 to 2001

#### Design Methodology Engineer in the Standard Storage Products Group

- Responsibilities included evaluation, recommendation, and implementation of current and future design methodologies pertaining to front end tools such as Verilog simulation and their interface to backend tools.
- Provided general ECAD support with emphasis on providing technical support for the Cadence Verilog-XL and NC-Verilog simulators as well as development of various PLI and VPI based utilities using C.

### Cadence Design Systems — Colorado Springs, Colorado — 1996 to 2000

#### Technical Services Group (TSG) Engineer

- Senior level AE providing expert level support, test, and debug of advanced customer issues for all Cadence Verilog-XL and NC-Verilog tools as well as the Verilog PLI and VPI interfaces.
- Responsible for development and delivery of advanced training materials for internal AE mentoring and training on Verilog tools as well as PLI and VPI programming.

- Provided departmental coordination between Support, R&D, Product Engineering, Product Marketing, and Product Validation groups within Cadence.

#### Field Applications Engineer

- Senior level field AE providing customer support for all Cadence Verilog HDL based tools. Included hot line support, on site customer visits, and extensive customer support for the NC-Verilog beta test roll out.

### Ford Microelectronics, Inc. — Colorado Springs, Colorado — 1984 to 1996

#### ECAD Engineer

- Responsible for user, system, and application support for the Verilog-XL simulator from gate through RTL and behavioral level.
- Responsible for definition and implementation of FMI proprietary Verilog standard cell model libraries.
- Responsible for custom internal C based PLI extensions to the Verilog language including: Vertical Header; GRANY Data Capture; Update Timing; Update Timing Checks; Check Module Paths.
- Participated in the Reusable IC Verification Environment (RIVET) team including definition and creation of Verilog simulation fixtures and their corresponding PLI interfaces to allow Verilog/C++ co-simulation.
- Participated in the definition and implementation of a full behavioral level Verilog model of the Hosted Bus Controller Chip (HBCC) using the Ford Standard Corporate Protocol (SCP) serial interface.
- Responsible for maintenance and enhancements of a custom internal C based application called the Standard Corporate Protocol Simulation Compiler (SCPSC) which was used as a front end to generate a complete Verilog simulation environment for networks of SCP based ICs.
- Responsible for specification and implementation of several internal EDA utilities. C based utilities included: Sentry to Zycad Stimulus Converter; Reliability Data Extraction Utility. Pascal based utilities included: 806X Microcode Minimization Program; 806X HILO PLA Model Generator; 806X Zycad PLA Model Generator; 806X PLA Layout Data Generator; 806X ROM Data Generator; Modular Simulation Stimulus Converter.
- Responsible for definition and implementation of a network of UNIX based engineering workstations including full and part time system administration.

### Martin Marietta Aerospace — Denver, Colorado — 1981 to 1984

#### Digital Design Engineer

- Digital Design Engineer assigned to the Flight Data Systems section, Logic Circuits Design Group.
- Provided engineering support and development for an ECAD system using the TEGAS-5 digital simulator.
- Designed a satellite power system controller implemented using CMOS SSI and MSI technology.
- Assisted in design, testing, and analysis of a 10-MHz Manchester PCM data bus realized in TTL logic. This included both laboratory testing and design verification using the TEGAS-5 simulator.
- Designed and developed TTL logic circuits for an 8085 based Control and Monitor System (CMS) which was an integral part of the MX missile launcher electronic hardware.

### Education, Specialized Training, Additional Skills

**Formal Education:** Bachelor of Science in Electrical and Electronic Engineering Technology (EET), March 1981, Montana State University, Bozeman, Montana. Overall GPA: 3.02 (A = 4.00).

**Specialized Training:** *Advanced C Programming* (University of Maryland); *Object Oriented Design with C++* (Ford Microelectronics); TestBuilder (Cadence); SystemC Fundamentals (Cadence); Introduction to SystemVerilog for Verification (Doulos); Class Based SystemVerilog Verification (Doulos); AVM Adopter (Doulos).

**Business Applications:** Microsoft Office: Word, Excel, PowerPoint, Visio. Technical publication: FrameMaker. Email applications: Outlook, Entourage, Eudora, Zmail, Sun MailTool, MacOS X Mail. Calendaring applications: Outlook, MeetingMaker, Mac OS X iCal. Database applications: FileMaker Pro, Panorama.