

ROBERT S. HOFFMAN

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ENGINEERING DESIGN MANAGER

Accomplished Engineering Design Manager with emphasis in Digital Design and Firmware. Extensive experience in digital design and firmware, project definition, best practice design techniques and management. Twenty five years of experience in engineering.

- Verilog RTL Digital Design
- Design Verification
- Firmware Development
- FPGA Design
- Design Prototyping
- VHDL Conversion to Verilog
- Project Management
- Work Breakdown Schedule
- Department Management
- Architecture Definition
- Design Flow Definition
- Design Automation

Excellent track record in leadership, communication, resource management, accountability and team building. Experience in leading a multi-site team. Experience with industry standard tools and design techniques.

- Cadence Virtuoso
- Verilog
- Mentor QuestaSim, Synopsys VCS
- Synopsys DC
- Xilinx ISE
- HSIM
- Microsoft Project, Access
- Microsoft Word, Excel, Powerpoint
- TCL, HTML, AWK, SKILL, C++, Shell Scripts
- Numerous other tools

PROFESSIONAL EXPERIENCE

Cypress Semiconductor, Colorado Springs, Colorado September '08 – Present ***Chip Architecture and RTL Design Contract Engineer / Project Lead***

Worked with a Cypress PSoC engineer to develop the architecture for embedding a Simtek nvSRAM macro in Cypress PSoC products. Defined the interface logic required to connect the macro to the PSoC system bus. Defined the architecture for an nvSRAM SPI interface and implemented the RTL. Created testbenches for the RTL. Ran and debugged integrated chip gate-level simulations.

Simtek Corporation, Colorado Springs, Colorado January '03 – September '08 ***Engineering Manager, Digital Design & Firmware***

Manage design of embedded digital control systems and other functions for non-volatile memory chips including microcontrollers, Real Time Clocks and IO interfaces. Design and development of test and emulation FPGA-based boards.

- Created Project Plans, WBS and schedule in Microsoft Project.
- Collaborated on the functional specifications.
- Collaborated on the development of a formal review procedures.
- Created a product lifecycle.
- Created project tracking forms.
- Created a department website to enhance communication.
- Developed a firmware development platform for rapid prototyping.
- Developed a low-cost application mode test system based on a Xilinx FPGA.
- Managed a dual site team of up to 10 engineers and engineering interns.
- Participated in the design.
- Moderated design reviews.

Simtek was purchased by Cypress Semiconductor in September 2008 and I became a Cypress contractor.

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Acculent Corporation, Colorado Springs, Colorado**January '02 – January '03****Co-Founder, Design Engineer, CEO**

Founded an intellectual property company and gained acceptance in the Colorado Springs Technology Incubator.

- Developed a methodology for the creation of highly-configurable Verilog RTL intellectual property.
- Created synthesizable code for DSP functions such as an FFT, FIR Filter, etc.
- Marketed intellectual property.
- Created a business plan, website, corporate image.
- Established a contracting relationship with Simtek Corporation.

Comsilica, Colorado Springs, Colorado**March '01 – November '01****Staff Engineer**

Lead engineer in the development of a PHY block for an IEEE 802.11a chip.

- Developed FFT, cordic processor, forward and inverse puncturing, predistortion compensator filter, DMA controllers, etc. in Verilog RTL.
- Validated design with Verilog and C programs.
- Managed the development of the PHY.
- Contributed to the functional specification.

(Company lost funding due to Sept. 11th and closed in November 2001)

Atmel Corporation, Colorado Springs, Colorado**June '97 – March '01****Senior Principal Design Engineer**

Lead engineer in the development 2nd generation cryptography chip and 2nd generation RFID chip.

- Took over RFID project and redesigned logic in Verilog RTL to remove bugs.
- Led a small group in the development of a 2nd generation cryptography chip.
- Wrote embedded firmware for I2C interface.
- Converted VHDL code to Verilog RTL.
- Created test benches to verify the design and to generate production test vectors.

Array Microsystems, Colorado Springs, Colorado**April '91 – June '97****Senior Design Engineer**

Gate-level design of a Discrete Cosine Transform block used in an Image Compression Coprocessor / Motion Estimation chipset. The chipset was used for high-end MPEG video compression.

- Gate-Level digital design from behavioral model.
- Design verification.
- Floorplanning, Place and Route of Image Compression and Motion Estimation chips.
- Automation of design flow with SKILL programming.
- Custom Standard Cell Library Development.
- CAD support.

Atmel Corporation, Colorado Springs, Colorado**Jan '90 – April '91****Senior Design Engineer**

Development of a CMOS standard cell library, BiCMOS testchip and CAD support.

- Standard Cell Library Development.
- Diva DRC Ruleset Creation.
- EPLD to Gate Array Conversions.
- Marketing Quotes.
- SKILL programming.
- CAD support.

Prisma Supercomputer, Colorado Springs, Colorado

Mar '89 – Nov '89

Senior Design Engineer

Development of custom GaAs logic chips for a supercomputer. Prisma was founded by former Cray Research employees to develop a pizza box sized super computer.

- Gate-Level Digital Logic Design from Behavioral Models.
- Auto and Manual Place and Route of custom logic chips.
- Development of High-Speed GaAs Standard Cell Library including circuit design, layout, SPICE characterization and logic modeling.
- Automated SPICE characterization program.
- Cadence Diva DRC rule set.

(Company shut down in November 1989)

Honeywell Solid State Electronics Division, Colorado Springs, Colorado July '83 – Mar '89

Senior Design Engineer

Design Engineer/Group Leader

Design Engineer

- Bipolar and RICMOS Gate Array Design – Senior Design Engineer
 - Project lead on a 1.25um bipolar gate array and 1.2um Radiation-Insensitive CMOS gate array.
 - Base layer and test chip design and characterization.
 - Gate Array Library Development including circuit design, layout, SPICE characterization and logic modeling.
- Library Development – Lead Design Engineer / Group Leader
 - Bipolar Gate Array Library Development.
 - Automated SPICE Characterization Program (Presented papers at CICC and GOMAC in 1987).
 - Supervised a group of five engineers and three technicians.
- Bipolar Gate Array Design – Design Engineer
 - Bipolar Gate Array Library Development.
 - Software Toolkit Strategy for maintaining timing and design information independent of technology.
- Engineering Training Program – Entry-Level Design Engineer
 - Product / Test Engineering – Test program review.
 - Process Engineering – Bipolar processing experiments on epitaxial layer.

EDUCATION AND CREDENTIALS

Bachelor of Science Degree in Electrical Engineering

COLORADO STATE UNIVERSITY – Fort Collins, Colorado, May 1983

Courses and Seminars

ASME Project Management for Engineers, Jan 2003

ADP Pay and Performance Seminar, Dec 2004

Read numerous books on project management.

Publications

Published four papers and presented two (CICC '87 and GOMAC '87)

Patents

Program Memory Test Access Collar, Patent Applied For, July 2007

PROFESSIONAL AFFILIATIONS

Member of IEEE

Member of Eta Kappa Nu