

Tim E. Fiscus, M.S.E.E.

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Experienced program manager, technical leader, and designer with proven success in development for small and large organizations worldwide.

EDUCATION: M.S. Electrical Engineering with concentration in Integrated Circuits, August 1996

National Technological University
G.P.A.: 3.15

B.S. Electrical Engineering with a Minor in Computer Science, August 1992

Penn State University, State College Pennsylvania
G.P.A.: 3.48

Pursuing B.S. Accounting – Enrolled in accounting degree program with a senior status

Youngstown State University, Youngstown Ohio
G.P.A.: 3.86

EXPERIENCE: Novocell Semiconductor

Hermitage, PA

9/08-Present

- Contracted with ON Semiconductor as a design engineer
 - EEPROM designer on 0.35um IP block design
 - Designed 11v charge pump system, test chip verification and design
- One Time Programmable (OTP) ROM and Serial IP block designer for memories ranging from 8bits to 1Kbits in 0.18um/0.13um technologies at Tower, UMC, IBM, and Jazz.

Cypress Semiconductor

Hermitage, PA

2004-9/08

Burlington, VT

2000-2004

- Program manager for the 0.13um 4M nvSRAM, 4M nvSRAM with RTC, and 1M nvSRAM with RTC/SPI which was a platform design in the new ONO technology at Cypress. The team included 40 engineers at two companies in seven centers around the world.
- Carried out the transfer of the PSRAM product line to ESMT which included design reviews, database transfer, enabling simulation and verification, test training, and customer return root cause.
- Established the design center and test lab in PA with two direct reports where I was also responsible for CAD, system administration, office management, and test engineering. The test lab included a MicroManipulator setup for picoprobng and a Mosaid 3480 tester.
- Technical Leader on the 0.12um ADMUX & MoBL PSRAM 3V/1.8V using thin oxide only devices that was the first design in this foundry technology. Led the team of 30 engineers at five design centers around the world.
- Technical Leader on the 0.17um 16M Address/Data Multiplexed (ADMUX) PSRAM. Worked with Nokia to define and design the first ADMUX PSRAM in the industry. This project won the 2004 new product of the year at Cypress.
- Designer on the 32M MoBL PSRAM design where I designed the state machine to hide the refresh, DRAM timers, test modes, address path, data path, command decode, and led the analog system team.
- Technical Leader on the 250MHz 4Mb NoBL/Sync SRAM that went through qualification with only a two layer mask change after tapeout.
- Analog Designer on the QDR SRAM where I designed a 400MHz analog DLL.
- Analog Designer on the 64M NoBL PSRAM where I designed the power system which included voltage regulators, voltage references, and charge pumps.
- Developed a DRAM design guideline specification

IBM's Microelectronics Division

Burlington, VT

1998-2000

- Designer on the 256Mb DDR DRAM design team with the responsibility of adding Double-Data Rate functionality and the clock path.
- Accomplishments were the clock path design and a 400MHz (200MHz clock) Digital DLL with a digital filter, fast lock acquisition, and a regulated tapped delay line.

Intel's Computing Enhancement Group

Chandler Arizona

1997-1998

- Analog/Mixed Signal Designer with a primary area of focus on phase-locked loops for frequency synthesis and clock recovery for serial communications.
- Accomplishments were a 200MHz differential 2x oversampling PLL / CRC for an 800Mb/s 1394 PHY, a 233MHz PLL and an 8bit current steering video DAC.
- Developed an analog CAD flow with my focus being the layout verification including LVS, DRC, and EXT using Dracula/Arcadia and Cadence's Diva.

IBM's Microelectronics Division

Burlington Vermont

1992 - 1997

- Technical Leader for 4Mb LP EDO DRAM and two follow on cost reduction designs that were qualified.
- Foundry interface for a joint alliance development with UMI for a cached DRAM. This work included detailed design reviews of the vendor's product and supervision of the design, characterization, qualification, test, and transfer to manufacturing.
- IBM representative in the SLDRAM consortium architecture group.
- DRAM IC designer responsible for array, IO, and analog block design/layout/simulation on Cadence tools.
- Performed silicon characterization and design debug using the MegaTester and IBM's PC tester.

SKILLS:

CAD

- IBM Internal tools (SLED, WED, GYM, & ASTAP), Intel Internal tools (TIM, CSE, DLS),
- Cadence (Composer, Analog Artist, Virtuoso, Diva, Dracula, Vampire, Spectre), Mentor Calibre, Avanti (HSPICE, Star-Sim, Star-RC, Hercules, Arcadia), Synopsys (Mill Tools w/ ACE, Nanosim), Silvaco SmartSpice, Antrim, Mathcad, Matlab.

Testers

- MegaTester (Unix Based PC Tester), Mosaid, and IBM PC Tester
- Module and Wafer bench testing with internal micro-probing.

Programming Languages

- Perl/PerlTK, TCL/TK, Ksh, Csh, C/C++, Awk, HTML