

Troy A. Meester

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Principal Digital Design Engineer, ASIC Design

B.S. Computer Engineering, Iowa State University

US Patent 6201731

Innovative Engineer with experience in engineering and management roles. ASIC design, design verification, functional specification, project management and business-management expertise are just a few these experiences. A complete understanding of current EDA (Electronic Design Automation) tools sets from industry leaders, Synopsys, Cadence, and Mentor Graphics to name a few. Logical and physical synthesis methodologies as well as the latest verification trends like System C, assertions and System Verilog are among the skills. Board level design and direct customer interaction experiences as an applications engineer round out a full system level approach to problem solving. Self motivated and managed, able to lead a design team as well as directly contribute to technical issues.

- ASIC Design Tools, Verification, and Synthesis
 - Cadence Design System
 - Mentor Graphics
 - Synopsys
 - ARC Cores
- FPGA Design
 - Xilinx, Altera, Lattice
- Analog and Mixed Mode Simulation
 - HSIM, HSIM Co-simulation
 - Questasim
 - Eldo
- Digital Design Tools/Environments
 - System Verilog
 - System C
 - Verilog
 - VHDL
- PCB Design
 - Mentor Expedition and DxDesigner
 - Cadence Orcad and Allegro
- Bench-top Equipment
 - Logic Analyzers
 - Oscilloscopes
- Operating Systems
 - Linux
 - Windows XP & Vista
 - Windows Server 2003 & 2008
- Software Development
 - Configuration Management (Synchronicity, CVS, IC Manage)
 - C, C++, JAVA, Perl
 - MySQL

Management

World Wide EDA Manager

- Directed Simtek's EDA environment purchasing ASIC design simulation/design workstations and servers based on Linux. Reconfigured existing EDA tool contracts with Synopsys, Cadence and Mentor Graphics. Estimated 50% increase in productivity..
- Created and integrated a remote design center in Dresden Germany doubling the companies engineering staff.
- Setup San Diego and Chengdu China design centers to support Agiga Inc., a wholly owned subsidiary of Simtek.
- Integrated design methodologies between Cypress Semiconductor and Simtek Corporation to allow joint development of nvSRAM. Allowed Engineering team to work around the clock in 4 different time zones.

Technical Marketing Manager

- Managed the application support group for Simtek's nvSRAM product line. Doubled design wins during the first year by providing one-on-one design consulting to Simtek's top 10 customers including Dell, HP and IBM.
- Delivered web based applications notes on best design practices for nvSRAMs
- Successfully introduced and won designs for Simtek 1 Mbit nvSRAM and 1Mbit nvSRAM with RTC.

Simtek/Cypress Transition Team

- Managed the shutting down of the Dresden operation of Cypress. Equipment and design data was transferred back to Colorado Springs and made available within the Cypress operation.
- Managed the IT aspects of closing the Simtek operation in Colorado Springs and migrating the existing equipment, services and data into the COS operation of Cypress.
- Managed the transfer of EDA/CAD and IT responsibilities of Agiga to Cypress making Agiga into a stand alone operation supported by Cypress.

Project Management

- Managed a software development team of 5 members to deliver logic mapping and architecture matching of Synthesized Boolean equations to PLA/PLD and FPGA devices.

Engineering**ASIC Design**

- Developed a SPI (Serial Peripheral Interface) and control state machine capable of operating at a clock rate of 40MHz as the interface for a SONOS nvSRAM. The design was delivered to be taped-out in 8 weeks.
- Integration of a digital controller with analog blocks embedded within an nvSRAM. Developed a mix-signal simulation environment based on HSIM and Questasim.
- Working knowledge and experience with analog blocks including charge pumps, level shifters, voltage references, reset circuits and oscillators.
- System Verilog training and certification course complete through Doulos.
- Design configurations of the ARC core processors to support of a single MAC/PHY hybrid chip for 802.11a.
- Lead Engineer in development of a wireless RFID tag controller to interface a 1K-bit Ferro Electric memory.
- Configuration and Synthesis of ARC Core VHDL soft core for control functions on a DSL soft core modem.
- Verification Engineer using System C, Verilog and VHDL mixed mode support for Cadence Design Systems.
- Verification Engineer developing, test benches and regression testing methodologies for repeatable simulation/verification results for nvSRAM memories.

FPGA Design

- Xilinx emulation board for nvSRAM. This capability allowed us to re-target existing Verilog implementations of nvSRAM controller logic on to a bench top environment for evaluation.
- Xilinx nvSRAM test environment. Allowed extensive power up, brown out and power down evaluation of nvSRAM design. This translated into valuable design recommendations for customer applications.

Electronic Hardware Design

- HP 16520/16521 50Mvector/s pattern generation stimulus board module for a Logic Analyzer.
- HP 1652B 100MHz/400MSa/s Oscilloscope Logic Analyzer product
- PC Board design with Mentor Graphics Expedition and DxDesigner tools.

Software Architecture/Design

- Logic Synthesis tool for Programmable logic development to compile HDL into Boolean equations.
- Device fitter software to match Boolean logic to PLA/PLD device architectures.
- Database and EDA tool integration for programmable logic support.

IT/Network Configuration

- Linux and MS Windows XP workstation methodology to support engineering ASIC development.
- Deployed Virtual Private Network (VPN) implementation to allow for engineering at remote sites.
- VNC (Virtual Network Computing) methodology to allow for inexpensive workstations and remote computing.
- Developed the Engineering web site at Simtek. Tied together design documentation and other engineering related documents and resources to internal web site. JAVA, Perl scripting, PHP and MySQL databases on Apache web servers was used.

Employment History**Cypress Semiconductor, Colorado Springs, CO Oct 2008 – Mar 2009**

EDA Manager: Simtek/Cypress Transition Team

Simtek Semiconductor, Colorado Springs, CO May 2004 – Sep 2008

Deputy to the VP of Engineering EDA Manager: World Wide Operations Technical Marketing Manager

T & T Consulting, Colorado Springs, CO October 2002 – May 2004

Principal Engineer Owner/Operator

Celis Semiconductor, Colorado Springs, CO October 1997 – February 2001

Principal Engineer Program Manager EDA/IT Manager

Diba Incorporated, Colorado Springs, CO Sept 1996 - June 1997

Staff Engineer

MINC Incorporated, Colorado Springs, CO 1988 - Sept 1996

Manager: Programmable Devices Sr. Software Engineer

Hewlett-Packard, Colorado Springs, CO 1984-1988

Development Engineer