

# Christopher L. Smith

2002 King Dr.  
Hermitage, PA 16148

Available for Relocation

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## QUALIFICATIONS SUMMARY

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**Experienced Circuit Design Engineer and Technical Leader with significant background in design, test, and validation of Integrated Circuits. Extensive experience and qualifications in all facets of the product life cycle, from initial feasibility analysis and conceptual design through documentation, design, validation, and characterization.**

## OBJECTIVE

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**To obtain a design, test, software development, or verification career with a stable company that provides world class quality in designing, testing and verification of their products.**

## TECHNICAL SKILLS

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**CAD:** Cadence Composer; Virtuoso; Mentor (Eldo, Calibre); Synopsys (Nanosim, VCS, DC, Tetramax); Simutest Verifier; Syntest TurboFault; Questasim / Modelsim;  
**OS:** UNIX (SunOS/Solaris); LINUX(RedHat); Windows (98/NT/2000/XP/Vista)  
**Business:** MS Office; MS Visio; MS Access; Adobe;  
**Development:** Perl; C; C++; TCL; Basic; CSH; mySQL; Verilog HDL

## PROFESSIONAL EXPERIENCE

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### STAFF DESIGN ENGINEER – CYPRESS SEMICONDUCTOR

06/2001 to 04/2009

Responsible for design, integration, verification, test, and characterization of memory products (**over 50 million transistors per design**).

#### Custom Circuit Designer (Transistor Level Design / Schematic Entry)

- Integrated chip level schematics for Address and Data Multiplexed Pseudo-SRAM (PSRAM) design
- Identified and implemented test mode design for PSRAM designs
- Developed an analog Self Refresh Oscillator that used a voltage proportional to absolute temperature
- Designed Voltage Proportional to Absolute Temperature (VPTAT) circuit that did not vary with process or external voltage.
- Defined Address Path for PSRAM products

#### Verification / Validation

- Developed system level verification methodology that was used to achieve and to increase 1<sup>st</sup> Pass Yield
- Worldwide Technical Lead in Product Verification with diverse and geographically distributed design teams
- Used strength modeling to reduce the number of behavioral models implemented and in so doing increased the logic coverage for the entire design
- Used Design of Experiments with Process, Voltage and Temperature (PVT) parameters to create a Datasheet Calculator which was used for model to silicon correlation

#### RTL Developer

- Defined and led the development of SPI RTL block that interfaced with a NVSRAM.
- Verified RTL and synthesized gate netlists at block and system level to guarantee no logic errors and to increase 1<sup>st</sup> Pass Yield on Silicon.
- Managed the quality and validity of the synthesis constraints

## PROFESSIONAL EXPERIENCE

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### **STAFF DESIGN ENGINEER – CYPRESS SEMICONDUCTOR (continued) 06/2001 to 04/2009**

#### **Design For Test**

- Achieved 99.5% or higher Stuck At Fault (SAF) Coverage on three NVSRAM Products thereby decreasing the Parts Per Million (PPM) Defect Rate to less than 2 PPM
- As a member for the Design For Test (DFT) Center of Excellence, led and improved quality, and testability on each design
- Converted and Verified Automated Test Patterns which reduced tester debug time
- Improved Fault Grading execution by automating the simulation process and decreasing Total Cycle Time
- Created Automated Manual Fault Simulation script for software BIST which improved SAF Coverage

#### **Test and Characterization**

- Verified and Documented Characterization and Test Procedures for Memory Products (SRAM Data Retention, Testmode Entry, Wafer Level Burn In, STORE and RECALL of NV cells, Low and High Voltage testing of the SRAM)
- Wrote Test Programs for the MOSAID 3400 Memory Tester.
- Developed Pattern and User Code for MOSAID 3400 Memory Tester in C++
- Championed, debugged, and suggested circuit fixes for SRAM related issues on NVSRAM products
- Tracked down excessive current in low power part by systematically characterizing each block of the device, and using Failure Analysis tools to identify the hot spots.
- Led cross functional NVSRAM Burn-In team to develop Wafer Level and Package Level Burn-In firmware algorithm.
- Developed Power Supply Break the Part Tester GUI using TCL/TK.
- Wrote NVSRAM test and characterization procedures in both TCL/TK and C++

#### **Other Accomplishments**

- Led Verification and Validation teams to achieve zero logic defects and achieve gross functional silicon
- Improved Testability and Reliability of designs by following company and industry specifications
- Wrote 3 Patents, 2 accepted and 1 pending
- Wrote over 400 technical memos to help communicate and to document procedures and results
- Determined and Wrote Design guidelines and specifications from external customer specifications
- Received Memory and Image Division Achievement Award for Excellence in Non-Volatile SRAM projects

### **COMPUTER INSTRUCTOR – BUTLER COUNTY COMMUNITY COLLEGE 01/2005 to 05/2006**

Responsible for instruction of Microsoft Word, Microsoft Excel, Microsoft PowerPoint, and basic computer knowledge. Prepared and administered lab exercises and tests, as well as, lectures.

### **ASSISTANTSHIP – PENN STATE APPLIED RESEARCH LAB**

**05/2000 to 05/2001**

Responsible for maintaining network database in MySQL. Wrote Object Oriented Perl for Network Protocols, such as, DNS, SNMP, and ARP.

### **LAB CONSULTANT – CENTER FOR ACADEMIC COMPUTING**

**08/1999 to 05/2001**

Responsible for administering computer labs at The Pennsylvania State University. Answered user questions and concerns and helped to maintain the operation of the lab.

## EDUCATION

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B.S. in Computer Science and Engineering – THE PENNSYLVANIA STATE UNIVERSITY – G.P.A. 3.3/4.0 – May 2001

## AFFILIATIONS

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**Professional:** Design for Test Center of Excellence; Semiconductor Product, Test and DFT; VLSI Design for Test; Semiconductor Professional's Group

**Community:** Deacon Board Covenant Presbyterian Church, President, Past Vice President; Volunteer Youth Leader; Head Football Coach for Pee Wee football

## PATENTS

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Christopher L. Smith, and David Chapman, Reducing Crowbar Current in Latch Hysteresis Receiver, US Patent #7,064,596

Christopher L. Smith, David Chapman, and Timothy Fiscus, Power Supply Detecting Input Receiver Circuit and Method, US Patent #6,970,032

## ENDORSEMENTS

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**Program Manager and Lead Design Engineer:** “Chris is a detail oriented design engineer. He has a broad range of skills that enables him to be the cornerstone of every project he works on. He has the capability and experience to take on analog or digital designs and is able to own the design flow from product definition through production. He has been the key go to guy for most difficult tasks on every project. A couple key accomplishments where: - Owned/developed the digital DFT flow and methods - Owned/developed the digital verification flow and methodology - Root caused several silicon issues using ebeam, hypervision, FIBs and testing He has a great work ethic which is hard working, communicates, takes on additional responsibilities, and completes his work on schedule.”

Tim Fiscus, Program Manager and Lead Design Engineer, Cypress Semiconductor

**Sr. Design Director:** “Chris is an enthusiastic, detail oriented design engineer who has assembled a broad range of skills that allows him to work relentlessly on critical path tasks enabling chip integration. Chris is always open to acquiring new skills and expanding his knowledge base. Chris has been key engineer during debug phase allowing acceleration of time-to-market and product introduction into volume production.”

Klaus Schuegraf, Sr. Design Director, Cypress Semiconductor

**Design Engineering Director:** “Chris is a dedicated employee who is always willing to do what he is asked. He is well rounded with experience in digital RTL design and simulation, design for test, digital custom circuit design, and NVSRAM architectures. His projects within the past year have included SPI block definition and RTL, DFT closure on three chips (scan insertion, fault grading, ATPG), chip level logic verification, NVSRAM ground rules definition, and chip level debug. He is very hard working and attentive to his milestones. He is easy to manage and professional in his communication, both with his peers and with his management. He also embraces the Cypress culture and strives to be a good corporate citizen.”

David Still, Design Engineering Director, Cypress Semiconductor